DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Scheme of Instruction
and
Syllabi of

IV/IV B.E. I and II Semesters

2014-2015

UNIVERSITY COLLEGE OF ENGINEERING
(AUTONOMOUS)
OSMANIA UNIVERSITY
HYDERABAD – 500 007, TELANGANA

Scheme of Instruction and Examination
B.E – IV Year (ECE)
Semester I

S. No	Code No.	Subject	Scheme of Instruction		Scheme of Examination			Credits
			L/T	D/P	Duration in Hours	Maximum Marks		
						Univ. Exam	Sessional	
	THEORY							
1.	EC 401 UE	Embedded System Design	4	-	3	75	25	4
2.	EC 402 UE	VLSI Design	4	-	3	75	25	4
3.	EC 403 UE	Microwave Techniques	4	-	3	75	25	4
4.	EC 404 UE	Data Communication & Computer Networks	4	-	3	75	25	4
5.		Elective II	4	-	3	75	25	4
	PRACTICALS							
1.	EC 431 UE	Microwave lab	-	3	3	50	25	2
2.	EC 432 UE	Electronic Design and Automation (EDA) Lab	-	3	3	50	25	2
3.	EC 433 UE	Project Seminar	-	3	-	-	25	2
	DEPARTMENTAL REQUIREMENT							
1.	SI 400 UE	Summer Internship	-	-	-	-	*Grade	2
		TOTAL	**20**	**9**	**--**	**475**	**200**	**28**

*S/A/B/C/D/E

Elective II

EC 405 UE	Digital Signal Processor & Architecture
EC 406 UE	Computer Organization and Architecture
EC 407 UE	Artificial Neural Networks
EC 408 UE	Satellite Communication
BM 406 UE	Medical Instrumentation (BME)
CS 408 UE	Data Base Systems (CSE)
EE 405 UE	Optimization Techniques (EEE)
ME 409 UE	Entrepreneurship (Mechanical)

EC 401 UE

EMBEDDED SYSTEM DESIGN

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To gain knowledge to design embedded systems.
- To understand the processor selection criteria for Embedded System Design.
- To gain the knowledge of tool chain for embedded systems.
- To get familiar with the ARM embedded system.

Unit I

Introduction To Embedded Systems: The Embedded Design Life Cycle - Product Specification, Hardware/Software Partitioning, Iteration And Implementation, Detailed Hardware And Software Design, Hardware/Software Integration, Product Testing And Release, Maintenance And Upgradation.

Unit II

The Selection Process: Choosing The Right Processor, Packaging The Silicon, Silicon Economics, System-On-Silicon, Adequate Performance, Performance Measuring Tools, Meaningful Benchmarking.

Unit III

Embedded Software Development Tools: Host And Target Machines, Cross Compilers, Cross Assemblers, Tool Chains, Linkers/Locators For Embedded Software, Address Resolution, Locator Maps.

Unit IV

Getting Embedded Software Into Target System: PROM programmer, ROM emulator, In Circuit- Emulators, Monitors, Testing On Your Host Machine - Instruction Set Simulators, Logic Analyzers, Software-Only Monitors.

Unit V

ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, ARM processor fundamentals, registers, current program status register, pipeline, exceptions, interrupts, and vector table, core extensions, architecture revisions, ARM processor families.

Suggested Reading:

1. David E. Simon, *An Embedded Software Primer*, Pearson Education Asia, 2006.
2. Andrew Sloss, Dominic Symes, Chris Wright, *ARM System Developer's Guide: Designing and Optimizing System Software* , Elsevier, 2004.
3. Arnold S Berger, *Embedded Systems Design*, South Asian edition, CMP Books, 2005.

EC402 UE

VLSI DESIGN

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To provide a perspective on Digital Design in the Deep Sub-micron Technology.
- To focus on CMOS and Bi CMOS Short-channel Transistor Models.
- To Study CMOS Inverter elaborately.
- To explore static and dynamic implementations of combinational and sequential circuit designs and introduce Testability of VLSI circuits.

Unit I

Design Abstraction in Digital circuits, Fabrication process flow of nMOS and pMOS transistors, Overview of CMOS and BiCMOS technologies, MOSFET Transistor under static conditions, channel Length Modulation, Velocity Saturation, Sub-threshold Condition, Threshold variations, MOS structure Capacitance, CMOS Latch up, Technology scaling.

Unit II

CMOS Inverter, Voltage Transfer Characteristics, Static Power Consumption, Dynamic Power Consumption, Propagation Delay, Power-Energy and Energy-Delay Product, Layout Design of basic gates, Silicon on Insulation Technology.

Unit III

Designing Combinational Logic gates in CMOS: Complementary CMOS, Ratioed Logic, Pass Transistor Logic, Dynamic CMOS logic-basic principle, Signal integrity issues in Dynamic Design, domino logic, np-CMOS logic, Merits and Demerits of above logic styles. Designing sequential logic: Bistability Principle, Multiplexer based latch, Dynamic latch, Pipelining.

Unit IV

Designing Arithmetic Building Blocks: Adder, Binary Adder, Full Adder, Mirror Adder, Transmission gate based Adder, Manchester Carry Chain Adder, Carry Bypass Adder, Carry Look ahead Adder, Carry Save Adder, Multiplier, Carry Save Multiplier, Barrel Shifter, Logarithmic Shifter. Design of Memory Structures: ROM cells, PROM, EPROM, EEPROM, Flash Memory, SDRAM and DRAM.

Unit V

Implementation of strategies for Digital ICs, Testing of VLSI circuits: Test procedures; Design for Testability- Ad Hoc Testing, Scab Based testing, Boundary Scan Design, Built in Self Test, Built-in logic block observer, Test Pattern Generator, Automatic Test Pattern Generation (ATPG).

Suggested Reading:

1. JAN.M. Rabaey, A. Chandrakasan and B. Nikholic, *Digital Integrated Circuits – A Design Perspective*, 2nd Edition, PHI, 2007.
2. David A Hodges, H. Jackson and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd Edition, Tata McGraw Hill, 2007.
3. John. P. Uymera, *Introduction to VLSI Circuits and system*, student edition, John Wiley and Sons, 2003.

EC 403 UE

MICROWAVE TECHNIQUES

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To learn field calculations between parallel planes and rectangular wave guide.
- To study and understand various microwave devices and circuits.
- To study the construction and to understand principal of amplification/Oscillation at microwave frequency.

Unit I

Waves between parallel planes, TE, TM, TEM Waves characteristics, Velocity of propagation, Group and Phase velocity, Wave Impedance, Attenuation in parallel plate guides.

Unit II

TE & TM Waves in rectangular wave guides, Wave impedance, Attenuation and Q of Waveguides, Waveguide resonators, Power handling capability, Transmission line analogy, Waveguide Design/Bandwidth.

Unit III

Microwave circuit concepts, Normalized voltage and current, Scattering parameters, properties of S- Matrix, Unitary property. S-Matrix for directional coupler, Magic tee, Construction, principle and applications of Attenuator, Phase Shifter, Circulator, Isolator, S-Matrix of Circulator.

Unit IV

High Frequency limitations of conventional tubes, Two cavity Klystron, Bunching by velocity modulation, Small signal theory of bunching, Effect of grid interception and de-bunching. Trans admittance, Reflex Klystron, Mathematical theory of bunching, Admittance spiral and condition of oscillation.

Unit V

Principle of operation, construction and characteristics of (1) Multi-cavity magnetron (2) TWT Amplifier and (3) Backward wave oscillator (qualitative treatment only), Microwave Solid-state devices: Introduction, Classification and Applications. TEDs —Introduction, Gunn Diode — Principle, RWH Theory, Characteristics, Basic Modes of Operation, Oscillation Modes.

Suggested Reading:

1. Samuel Y. Liao, *Microwave Devices and Circuits*, 3rd Edition, PHI, 1994.
2. Pozar D.M., *Microwave Engineering*, 3rd edition, John Wiley & Sons, 2005.
3. Skalnik, Krauss, Reich, *Microwave principles*, East West Press, 1976.

EC 404 UE

DATA COMMUNICATION AND COMPUTER NETWORKS

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To understand the basic protocols of communication Networks.
- To familiarize the student with basic Taxonomy and terminology of computer networks.
- To expose the student to advanced Networks design and maintenance of computer network.

Unit I

Introduction to communication networks, Design principles for Communication Networks, Network services and architecture, Layered Network architectures, classes of communication services, protocols and standards, The OSI model, The TCP/IP model.

Unit II

Physical layer, Signal propagation, Optical bit transmission, Transmitting bits with radio and transmission lines, Synchronization and framing, Error control, Data link layer, Data link protocol, Alternating bit protocol, selective repeat protocol, Go back N protocol.

Unit III

Local area networks, ALOHA protocol, Ethernet and 802.3,Token Ring network, Token Bus network, FDDI,DQDB,WLAN 802.11,HYPERLAN,802.16,Bluetooth,Connecting LANs, Connecting devices, Backbone networks.

Unit IV

Switching, multiplexing, Network layer Names and address, Routing, congestion control, Network design, Transport layer, TCP,UDP and TP4, Session layer, Encryption, public key cryptography, Data compression, Syntax Conversion.

Unit V

Application layer, Integration of services, Hierarchy of telephone network, ISDN, Broad band ISDN, Introduction to ATM, ATM switches, Network simulation and protocol analyzer (Advanced Design system Software).

Suggested Reading:

1. Jean Walrand, *Communication Networks*, 1st edition, Irwin publications, 2002.
2. Behrouz A. Farouzan, Sophia Chang Fegan, *Data communication and Networking*, 4th Edition, McGraw Hill, 2004.
3. Andrew S Tanenbaum, *Computer Networks*, 4th edition, Pearson Educations, 2004.

EC 431 UE

MICROWAVE LAB

Instruction:	3 Periods per week
Duration of University Examination:	3 Hours
University Examination:	50 Marks
Sessional:	25 Marks
Credits	2

Objectives :

- To verify the various Characteristics of Active and Passive Microwave Devices Practically.
- To Measure Different parameters of an Antenna.
- To find Practically Optical Fiber Characteristics.

List of Experiments

A. Microwave Source Characteristics

1. Reflex Klystron Characteristics
2. Gunn diode Characteristics

B. Waveguide, Component Characteristics

3. Measurement of standing wave pattern, VSWR measurement, Low & High VSWR measurements
4. Measurement of Frequency, wavelength, group and phase velocity.
5. Measurement of an unknown load characteristics of windows.
6. Directional Coupler Characteristics, Coupling, Directivity. and Isolation Measurements.
7. E plane, H plane and Magic Tee characteristics.
8. Characteristics of Circulator, Isolator, Measurements of S-parameters through insertion loss and isolation.

C. Antenna Characteristics

9. Measurement of principle plane radiation patterns for horn, Yagi Uda, folded dipole.
10. Measurement of gain & input impedance.
11. Linear array characteristics.

D.OPTICAL COMMUNICATION

1. Optical Transmitter & Receiver Characteristics (Source & Detector) Analog/Digital Transmission link characteristics
2. Optical Fiber Characteristics: Attenuation, Numerical aperture, splicing losses (step & graded index).
3. Modulation & Demodulation Techniques

Suggested Reading:

1. Samuel Y. Liao, Microwave Devices and Circuits, PHI, 3rd Edition, 1994.
2. Pozar D.M., Microwave Engineering, John Wiley & Sons 3 rd edition,2005.

EC 432 UE

ELECTRONIC DESIGN AND AUTOMATION LAB

Instruction	3 periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessionals	25 Marks
Credits	2

Objectives:

- To understand the programming constructs of Verilog HDL.
- To demonstrate the programming models of Verilog HDL: gate level, data flow, behavioural and structural modelling.
- To study the VLSI back end tools
- To develop basic models of digital circuits using VLSI back end tools.
- To carry out mini projects using Verilog HDL.

List of Experiments:

Part A

Write the Code using VERILOG, Simulate and synthesize the following:

1. Arithmetic Units: Adders and Subtractors.
2. Encoders, Decoders, Priority Encoder and Comparator.
3. 8 – Bit Parallel Adder using four bit tasks and functions.
4. Arithmetic and Logic Unit with minimum of eight instructions.
5. D, SR and JK Flip flops.
6. Registers/Counters.
7. Sequence Detector using Mealy and Moore type state machines.

Note:

1. All the codes should be implemented appropriately using Gate level, Dataflow and Behavioural Modelling.
2. All the programs should be simulated using test benches.
3. Minimum of two experiments to be implemented on FPGA/CPLD boards.

Part B

Transistor Level implementation of CMOS circuits

1. Basic Logic Gates: Inverter, two input NAND and NOR gates.
2. Half Adder and Full Adder.
3. 4:1 Multiplexer.
4. 2:4 Decoder.

General Note: Mini Project cum Design exercise:

The student must design, develop code and test and design the following problems:

i) 8 bit CPU
ii) Generation of different waveforms using DAC
iii) RTL code for Booth's algorithm for signed binary number multiplication
iv) Development of HDL code for MAC unit and realization of FIR Filter
v) Design of 4 - bit thermometer to Binary Code Converter

Suggested Reading:

1 Samir Palnitkar, "*Verilog HDL: A Guide to Digital Design and Synthesis*", Pearson Education, 2005.
2 Jan M Rabaey, A. Chandrakasan and B. Nikolic., *Digital Integrated Circuits,* Prentice Hall of India, 2003.

EC 433 UE

PROJECT – SEMINAR

Instruction:	3 Periods per week
Duration of University Examination :	Viva Voce
Sessionals:	Grade*
Credits	2

Objective of the project - seminar is to actively involve the students in pre-preparation of the final year project with regard to following components:

Problem definition and specifications

Literature survey, familiarity with research journals

Broad knowledge of available techniques to solve a particular problem

Planning of the work, preparation of bar (activity) charts

Presentation - oral and written.

The Department can initiate the project allotment procedure at the end of 3rd year 2nd semester and finalize it in the first two weeks of 4th year Ist semester.

First 4 weeks of 4th year 1st semester will be spent on special lectures by faculty members, research scholars PG students of the department and invited lectures by engineers from industries and R&D institutions. The objective of these preliminary talks will be to expose the students to real life practical problem, and methodology to solve the technical problem

Seminar schedule will be prepared by the coordinator for all the students from 5th week to last week of the semester which should be strictly adhered to

Each student will be required to

1. Submit one page synopsis before the seminar for display on notice board.
2. Give 20 minute presentation followed by 10 minute discussions.
3. Submit the technical write up on the talk

At least two teachers will be associated with the project seminar to evaluate the students for sessional marks on the basis of performance in 3 items started above.

Note: Three periods of contact load will be assigned to each project guide irrespective of number of projects.

SI 400 UE

SUMMER INTERNSHIP

Instruction:	
Duration of University Examination:	Viva-Voce
University Examination:	Grade*
Sessional:	50 Marks
Credits:	2

Industry Design Project is introduced as part of the curricula for encouraging students to work on problems of interest to industries. A batch of three students will be attached to a person from an Electronics Industry / R & D Organisation for a period of 8 weeks. This will be during the summer vacation following the completion of the III year Course. One faculty co-ordinator will also be attached to the group of 3 students to monitor the progress and to interact with the Industry Co-ordinator (person from industry)

After the completion of the project, students will submit a brief technical report on the project executed and present the work through a seminar talk to be organized by the Department. Award of sessionals are to be based on the performance of the student, to be judged by a committee constituted by the Department. One faculty member will coordinate the overall activity of Industry Attachment Programme.

*** S/A/B/C/D/E**

EC 405 UE

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To understand basic features of programmable DSP processor.
- To study instruction set and addressing modes of TMS 320C 54XX.
- To implement different algorithms by DSP processor.

Unit I

Introduction: Features of programmable DSP Processors, Comparison between DSP's and microprocessors, computational accuracy in DSP implementations - fixed point and floating point processors, dynamic range, sources of errors, the Q-Notation.

Unit II

Programmable DSP Processors (TMS320C54XX): Basic Architectural features, addressing modes including circular addressing and bit reversal addressing, memory space, interrupts, address generation units, program sequencer, pipe lining and parallelism.

Unit III

Instruction set of TMS320C54XX: Arithmetic, move, load/store, logical, control, special control instructions, I/O instructions, parallel instructions, instructions for bit manipulation and call instructions.

Unit IV

An overview of TMS320C6xx DSP's: Basic features, architecture, addressing modes, memory architecture and pipe line operation. Recent trends in DSP system design, overview of DSP system, FPGA based system design.

Unit V

Implementation of DSP algorithms: Matrix multiplication, convolution, correlation, FIR filters, RR filters, Decimation and interpolation filters. Implementation of PID controller and position control system for a hard disk drive system.

Suggested Reading:

1. Avatar Singh and Srinivasan. S, *Digital Signal Processing Implementations*, Thomson Books, Singapore, 2004.
2. Venkata Ramani. B and Bhaskar. M., *Digital Signal Processors — Architecture, Programming and Applications*, Tata McGraw Hill, New Delhi, 2002.
3. Imanuel C.Ifeacher, BW Juris, *Digital Signal Processing - A Practical Approach*, 2nd Edition, Pearson Edition, 2002.

EC 406 UE

COMPUTER ORGANIZATION AND ARCHITECTURE

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To familiarize with Register Transfer Language (RTL) and Micro-operation concepts.
- To demonstrate the design of Data Path and Control Units.
- To know IO processor and cache memory organization.
- To understand parallel processing concepts.
- To study operating systems fundamentals.

Unit I

Register Transfer Language and Micro operation: Introduction to Digital Systems using VHDL, Difference between Computer Organization and Architecture, Processor Organization, Coprocessor, RTL notation, Common bus system using multiplexer and tri-state buffers. Micro-operations: Arithmetic, Logical and Shift. Basic Computer Organization: Computer registers, instruction and Design of basic computer Basic Computer Organization: Computer registers, instruction and Design of basic computer. Instruction formats and Addressing modes.

Unit II

Computer Arithmetic: Fixed and floating point numbers: Adders: Binary adder, carry look ahead adder, Tree adders: Parallel prefix adder, Sparse Kogge-Stone adder and Spanning tree look ahead adder, Multiplication: Robertson's, Booth's algorithms, Array Multiplier and Wallace tree multiplication and HDL descriptions. Division: Restoring and Non-restoring algorithms and HDL descriptions, floating point arithmetic and BCD Adder, Shifter: Barrel shifter and Logarithmic shifter.

Unit III

Control Unit Design**:** Significance of Control unit, Hardwired Control unit design approach (classical and one-hot methods). Case studies: control unit designs of GCD processor, DMA controller and CPU. Micro-programmed Control unit approach: basic concept, micro-program sequencer. Case Study: CPU control unit.

Unit IV

Input Output and Memory Organization: Input-output interface, Modes of transfer, Priority interrupt, Input-Output Processor (IOP) Memory Organization: Memory hierarchy, Main memory, Shared memory, Cache memory, address mapping techniques, replacement policies

Unit V

Advances in Computer Organization: Parallel processing: Pipeline – Arithmetic and Instruction, Pipeline Conflicts, Vector processing, Array processing, VLIW architecture, Characteristics of Multi-processor system and super scalar concept Operating System Overview: Scheduling techniques, necessity of Real Time Operating System (RTOS).

Processor Performance enhancement strategies: Overlap, Scalar, Super-scalar, Super-pipeline, Instruction Level Parallelism (ILP), Processor Level Parallelism (PLP), Introduction to Message Passing Interface (MPI).

Suggested Reading:

1. Morris Mano M, *Computer System Architecture*, 3rd edition, Prentice Hall India, 2007.
2. William Stallings, *Computer Organization and Architecture*, *Design for Performance,* 7th edition, Prentice Hall India, 2006.
3. John P. Hayes, *Computer Architecture and Organization*, 3rd edition, McGraw Hill, 1998.

EC 407 UE

ARTIFICIAL NEURAL NETWORKS

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To understand the functioning of biological neuron and its electronic implementation.
- To learn different training algorithms in training neural networks.
- To understand the concepts of pattern recognition and pattern association as applied to neural networks.

Unit I

Description of biological neuron, Different neuron models, Mcculloch pitts neuron model, Perceptron and Adaline neuron, Basic learning laws: Hebb's law, Pesceptron, delta, widrow and Hoff LMS, correlation, winner take and outstar learning.

Unit II

Activation and synaptic dynamics of neural networks: Additive, shunting and stochastic activation models. Requirements of learning laws, Distinction between the activation and synaptic dynamics models several categories of learning methods. Recall in Neural networks.

Unit III

Different neural network models and their applications pattern association, pattern storage (LTM & STM), Pattern clustering and feature map, Neural network memory: Hetro associative, Interpolative and auto associative.

Unit IV

Feed forward neural networks, multi layer neural network with linear and non linear Processing units. Peceptron neural networks solution of xoR problem, pesceptron learning law. Pesceptron convergence theorem, Back propagation learning rule, Features of Back propagation, and limitations of and extensions of Back Propagation rule.

Unit V

Feedback Neural networks, Linear auto associative feed forward and feedback networks. Hopfield network, capacity and energy analysis of Hopfield neural network . Stochastic neuron, Boltzmann machine, Boltzman learning law, Issues in Implementation of Boltzman learning law.

Suggested Reading:

1. B. Yeganaranarana, *Artificial Neural Networks*, Prentice Hall, New Delhi, 2007.
2. J. A. Freeman and D.M. Skapura, *Neural Networks Algorithms, Applications and Programming Techniques*, Addison Wesley, New York, 1999.
3. Simon Haykin, *Neural Networks (A Comprehensive Foundation)*, McMillan College Publishing Company, New York, 1994.

EC 408 UE

SATELLITE COMMUNICATION

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Course Objectives

- To introduce basic principles of satellite communication.
- To study various components of a spacecraft.
- To understand the uplink and downlink design steps.
- To learn various modulation and multiplexing techniques for satellite links.

Unit I

Origin of satellite communications, Basic principles and properties of satellite communication. Earth segment, Space segment. Orbital mechanics and Kepler's Laws. Orbital effects in communication system Performance. Doppler shift, Range variation, Eclipse and sun transit outage.

Unit II

Space craft sub systems, System reliability and design life time, SAT launch and launch vehicles

Unit III

Earth Stations, Design of large antennas and small earth station antennas. Low noise amplifiers and High power Amplifiers for satellite communication.

Unit IV

System noise temperature and G/T ratio. Basic RF link analysis. Attenuation, depolarization, atmospheric absorption, Multipath effects, Faraday rotation and ionospheric scintillations, Rain and ice effects,

Unit V

Satellite Applications: INTELSAT, INSAT, INMARSAT, Satellite Navigational system and Remote sensing satellites.

Suggested Reading:

1. Wilbur L. Pitchand and Henri G. Suyderhoud, Robert A. Nelson, *Satellite Communication Systems Engineering*, 2nd edn.3rd Impression, Pearson Education.2008.
2. Timothy Pratt and Charles Nestian. W, *Satellite Communication*, John Wiley and Sons, 1988.
3. Tri T. Ha, *Digital Satellite Communication*, Tata McGraw- Hill, Special Indian Edition 2009.

Scheme of Instruction and Examination
B.E – IV Year (ECE)
Semester II

S.No	Code No.	Subject	Scheme of Instruction		Scheme of Examination			Credits
			L/T	D/P	Duration in Hours	Maximum Marks		
	THEORY					Univ.Exam	Sessional	
1.	EC 451 UE	Mobile and Cellular Communication	4	-	3	75	25	4
2.	ME 471 UE	Industrial and Financial Management	4	-	3	75	25	4
3.		Elective III	4	-	3	75	25	4
4.		Elective IV	4	-	3	75	25	4
1.	EC 481 UE	Project		6	Viva Voce	*Grade	50	12
2.	EC 482 UE	Seminar		3	-	-	25	2
	TOTAL		**16**	**9**	**-**	**300**	**175**	**30**

*Excellent/Very Good/Good/Satisfactory/Unsatisfactory

Elective III

1. EC 461 UE Real Time Operating system
2. EC 462 UE Fuzzy logic & Applications
3. EC 463 UE Design of Fault Tolerant Systems
4. EC 464 UE Radar Systems

Elective IV

1. EC 471 UE Global Navigational Satellite System
2. EC 472 UE Multirate Signal Processing
3. EC 473 UE CPLD and FPGA Architecture & Applications
4. EC 474 UE Advanced Topics in Microwaves

EC 451 UE

MOBILE AND CELLULAR COMMUNICATION

Instruction:	4 Periods per week
Duration of University Examination:	3 Hours
University Examination:	75 Marks
Sessional:	25 Marks
Credits	4

Objectives

- To know Wireless communication standards.
- To understand pathloss models.
- To understand different parameters of time and frequency dispersion.
- To understand characteristics of multi-path fading channels.

Unit I

The cellular concept: System design fundamentals, Frequency reuse, Channel Assignment strategies Handoff strategies, Power control, Interference and system capacity, Improving coverage and capacity in cellular systems, Basic cellular mobile communication system.

Unit II

Mobile radio propagation: Large scale path loss-Introduction to radio wave, Free space propagation model, Three basic propagation mechanisms, Reflection, Ground reflection (two ray) model) model, Diffraction, Scattering, Practical link budge design using path loss models, Outdoor propagation models, Indoor propagation models, signal penetration into buildings.

Unit III

Mobile radio propagation: Small scale fading and multipath — small scale multipath propagation, Impulse response model of a multipath channel, Small scale multipath measurements, Parameters of mobile multipath channels, Types of small scale fading, Rayleigh and Ricean distributions, Statistical models for multipath fading channels.

Unit IV

Equalization, Diversity, speech coding: Equalization in a communication receiver, Linear equalization, Non linear equalization, Algorithms for adaptive equalization, Diversity techniques, Rake receiver, Vocoders, Linear predictive coders, Choosing speech CODECs for mobile communications.

Unit V

Wireless systems and standards: Multiple access techniques for wireless communications — FDMA, TDMA, spread spectrum multiple access SDMA, Packet radio, CSMA, Reservation protocols, Evolution of wireless systems, Study of AMPS, 15-54, IS- 136, GSM, IS-95, CDMA-2000, WCDMA, Introduction to Multi User Detection, 4th Generation systems, Simulation Software for communication systems (Advanced Design System Software).

Suggested Reading:

1. Theodore S., Rappaport, Wireless Communications, Pearson Education, 2002.
2. V.K.Garg, IS-95 CDMA & CDMA 2000, Pearson Education, 2002.
3. William C.Y. Lee, Mobile Communications Engineering, McGraw Hill, Second Edition, 1998.

ME 471 UE

INDUSTRIAL AND FINANCIAL MANAGEMENT

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks
Credits	4

Objectives

- To understand various types of organizational structures, manufacturing processes and importance of plant layout and the role of scheduling function in optimizing the utilization of resources
- To understand the importance of quality, inventory control and concepts like MRP I and MRP II
- To understand the nature of financial management and concepts like breakeven analysis, depreciation and replacement analysis

Unit-I

Types of organizations, organizational structures.Designing Products, Services and Processes: New product design and development. Product life cycle: phasing multiple products. Manufacturing process Technology: Product, job shop, batch, assembly line and continuous process technology; flexible manufacturing systems.

Design of Services, service process technology operations capacity; capacity planning decisions, measuring capacity; estimating future capacity needs.

Unit-II

Locating production and services facilities, effects of location and costs and revenues, factor rating, simple median model (linear programming)

Layout planning; process layout; product layout — Assembly lines; line balancing manufacturing cellular layout.

Scheduling systems and aggregate planning for production and services; loading assignment algorithm; priority sequencing and other criteria.

Unit-III

Quality planning and Control: basic concepts, definitions and history of quality control. Quality function and concept of quality cycle.Quality policy and objectives.Economics of quality and measurement of the cost of quality.Quality considerations in design.

Process control: machine and process capability analysis. Use of control charts and process engineering techniques for implementing the quality plan. Acceptance sampling: single, double and multiple sampling, operating characteristic Curve - calculation of producers risk and consumers risk.

Unit-IV

Inventory control**:** deterministic and stochastic inventory models; variable demand; lead time, specific service level, perishable products and service.

Inventory control in application; concepts for the practioners; saving money in inventory systems; ABC classifications.

Inventory control procedures; Quantity - reorders versus periodic inventory systems; material requirement planning (MRP); MRP as a scheduling and ordering system; MRP system components; MRP computational procedure; Detailed capacity planning; MRP - limitation and advantages; Manufacturing Resources Planning (MRP-II).

Unit-V

Elements of cost, overheads, breakeven analysis, depreciation, replacement analysis. Nature of financial management-time value of money, techniques of capital budgeting and method, cost of capital, financial leverage.

Suggested Reading:

1. Buifa and Sarin, "Production and operations management" - Wiley Publications.
2. I.M. Pandey, "Elements of Financial Management" Vikas Publications, New Delhi, 1994.
3. James C. Van Home & John, M. Wachowicz, Jr., "Fundamentals of Financial Management", Pearson Education Asia, 11th ed. 2001.

EC 481 UE

PROJECT

Instruction	6 Periods /week Viva
Duration of University Examination:	Viva Voce
Sessionals	50 Marks
Credits	12

Solving a real life problem' should be the focus of U.G. projects. Faculty members should prepare project briefs well in advance which should be made available to the students at Departmental library. The project may be classified as Hardware, Software, Modeling, Simulation. It should involve one or "many elements of techniques such as analysis, design. Synthesis.

The Department will appoint a project coordinator who will coordinate the following

Grouping of students (a maximum of three in a group)

Allotment of projects and project guides
Project monitoring at regular intervals

All project allotments will be completed by the 2nd week of IV year 1st semester so that students get sufficient time for completion of the project

All projects will be monitored at least twice in a semester through student's presentation. Sessional marks should be based on the grades/marks awarded by a monitoring committee of faculty members and also marks given by the supervisor.

Efforts be made that some of the projects are carried out in industries with the help of industry coordinators. Problems can also be invited from the industries to be worked out through U.G. projects.

Common norms will be established for final documentation of the project report - by the respective Department .

Grades Note :
Excellent / Very Good / Good / Satisfactory / Unsatisfactory :
Three periods will be assigned to each project guide irrespective of number of projects.

EC 482 UE

SEMINAR

Instruction	3 Periods/week Viva
Sessional	50 Marks
Credit	2

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the student for a systematic and independent study of state of the art topics in road area of his/her specialization.

Seminar topics may be chosen by the students with the advice from faculty members. Students are to be exposed to following aspects of seminar presentations.

Literature survey
Organization of material
Preparation of OHP slides/PC presentation
Technical writing

Each student is required to

1. Submit a one page synopsis of the seminar talk for display on notice board.

2. Give a 20 minutes presentation through OHP, PC, slide projector, followed by 10mts discussion.

3. Submit a report on the seminar topic with list of references and slides used

Seminars are to be scheduled from 3rd week to the last week of the semester and any change in schedule should be discouraged.

The sessional marks will be awarded to the student by at least 2 faculty members on basis of an oral and a written presentation as well as their involvement in the discussions.

EC 461 UE

REAL TIME OPERATING SYSTEMS

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks
Credits	4

Objectives

1. To introduce Real Time Operating Systems
2. To familiarize the concepts of all Real Time Operating Systems
3. To understand the importance of RTOS in building real time systems
4. To get familiar with the standards like POSIX
5. To study a real time system with a view of porting an RTOS onto it.

Unit I

Real Time Systems : Jobs and processors, release times, Deadlines and timing constraints, hard and soft timing constraints, Hard real time systems, soft real time systems.

Unit II

Survey of software architectures: Round robin, round robin with interrupts, Function Queue scheduling, Real time operating system architecture, Scheduling Real-Time Tasks -Types of Schedulers, Table-driven scheduling, Cyclic schedulers, EDF, RMA , selecting an architecture,

Unit III

Introduction to Real Time Operating Systems: Tasks and task states, tasks and Data, Semaphores and shared data.Operating system services: Message queues, mailboxes and pipes, timer functions, events, memory management, Interrupt routines in an RTOS environment.

Unit IV

UNIX as Real-Time Operating System: Non-preemptive kernel, Dynamic priority levels, other deficiencies of Unix, Windows as Real time operating systems – Important features of windows NT, shortcomings of Windows NT, Windows NT versus Unix, POSIX – Open software, Genesis of POSIX, overview of POSIX, Real time POSIX standard.

Unit V

Survey of Contemporary Real Time Operating Systems: PSOS, VRTX, VxWorks, QNX, µC/OS-II, RT Linux, Lynx, Windows CE.

Suggested Reading

1. Jane W.S.Liu, " Real Time Systems", Prentice Hall, 2000
2. David E Simon, "An Embedded software primer", Pearson, 2012
3. Rajib Mall, "Real-Time Systems: Theory and Practice," Pearson, 2008.

EC 462 UE

FUZZY LOGIC AND APPLICATIONS

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks
Credits	4

OBJECTIVES:

- To learn the concepts of regular and fuzzy sets.
- To gain the knowledge to use fuzzy sets for different applications.
- To learn the different neural and fuzzy memories.

Unit I

Basics of Fuzzy sets: Fuzzy sets, operation on Fuzzy sets, Extensions of Fuzzy set concepts, extension principle and its applications. Geometry of fuzzy sets, sets as points, counting with fuzzy sets.

Unit II

Fuzzy Relations: Basics of fuzzy relations, operations on fuzzy relations, various types of Binary fuzzy relations, fuzzy relations equations.

Unit III

Membership Functions: Features of the membership function, fuzzification, Membership value assignments — In tuition, in science, Rank ordering, Neural Networks.

Unit IV

Fuzzy — to — crisp: conversions: Defuzzification methods — Max-membership principle, central method, weighted average method, mean-max membership, center of sums, center of largest area, first (or last) of maxima.

UnitV

Fuzzy Associative memories: Fuzzy systems as between — cube mappings, fuzzy and neural function estimators, neural Vs Fuzzy representation of structured knowledge, FANS as mappings, fuzzy Hebb FAMS, the bi-directional FAN theorem for correlation minimum encoding, correlation — product exuding, superimposing FAM rules, recalled outputs and defizzifaction, FAM structure Architecture. Binary input — output FAMS, example of Invented pendulum — Fuzzy contains crane control.

Suggested Reading:

1. C.T. Lin and C.S.George Lee, "Neural Fuzzy Systems", PHI, 1996
2. Bant A KOSKO, "Neural Nehvorks and Fuzzy Systems", PHI, 1994
3. Altrock, C.V., "Fuzzy Logic and Neuro Fuzzy Applications explained", PHI, 1995
4. Timothy J.Ross, "Fuzzy Logic with engineering Applications", McGraw —Hill, Inc. 1997.

EC 463 UE

DESIGN OF FAULT TOLERANT SYSTEMS

Instruction	4 periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessionals	25 Marks
Credits	4

Objectives

- To understand various methods for deriving economical fault detection and location test experiments and compare them.
- To be able to generate tests for fault detection and location in sequential circuits.
- To use coding techniques to generate test patterns using self checking circuits.
- To represent physical faults by logical faults and understand fault simulation methods.
- To address the problem of test generation for SSFs using TG algorithms.

Unit I

Fault detection and location in Combinational Circuits: Fault detection and location; classical methods- path sensitisation, ENF method, two level and multi level fault detection, Boolean difference method and Spoof method, detection of multiple faults, Kohavi method D-algorithm, singular covers, d-intersection.

Unit II

Fault Detection and Location in Sequential Circuits: Circuit test approach, initial state identification, final state identification, Design of fault detection, experiment for diagnosable machines.

Unit III

Self Checking Design: Basic concepts, application of Error-detecting and Error-correcting codes, multiple bit errors, checking circuits and self checking, self-checking checkers, parity-check functions, totally self checking m/n code checkers, totally self-checking equality checkers, self checkingberger code checkers, self checking sequential circuits.

Unit IV

Fault modeling and Simulation: Functional modeling at logic level, register level and structural level, logical fault models, hazards and hazard detection, fault simulation for combinational circuits, fault sampling.

Unit V

ATG for SSF and bridge faults in combinational circuits: Fault oriented ATG, fault independent ATG, random test generation, bridging fault model, detection of non feedback and feedback bridging faults, bridging fault simulation and test generation.

Suggested reading:

1. Samuel C Lee “Digital Circuits and Logic Design”. PHI Pvt. Ltd. 2000
2. ZviKohavi “ Switching and Finite Automata Theory”, TMH.2nd edition
3. M.Aframonici, M.Brerrer, A.Friedman, “ Digital System Testing and testable design”, Jaico publications

EC 464 UE

RADAR SYSTEMS

Instruction:	4 Periods per week
Duration of University Examination:	3 Hours
University Examination:	75 Marks
Sessional:	25 Marks
Credits	4

Objectives:

- To familiarize with different Radar Systems.
- To learn about Radar antennas.

Unit I

Radar Systems:Description of basic radar system and its elements, Radar equation, Block diagram and operation of a radar, Radar frequencies, Application of Radar, Prediction of range performance, Minimum detectable signal, Receiver noise figure, Effective noise temperature, Signal to noise ratio, False alarm time and probability of false alarm, Integration of radar pulses, Radar cross-section of target, Pulse-repetition frequency and range ambiguities, System losses.

Unit II

CW and FMCW Radars:Doppler effects, CW Radar, FMCW Radar, Multiple frequency CW radar, Low noise front-ends, A-scope, B-scope, PPI Displays, Duplexers.

Unit III

MTI and Pulse Doppler Radar:MTI radar, Delay line canceller, Multiple and staggered prf, Blind speeds, Limitations to MTI performance, MTI using range gated Doppler filters, pulse Doppler radar, Non coherent radar.

Unit IV

Tracking Radar:Sequential lobing, Conical scan, Monopulse-amplitude comparison and phase comparison methods, Tracking in range and in Doppler, Acquisition, comparison of trackers.

Unit V

Search Radar:Range equation, search scans, Effect of surface reflection, Line of Sight (LOS), propogation effects, Environmental noise. Radar Antennas: Antenna parameters- Parabolic reflector antennas, Cassegrain antenna, Cosecant - squared Antenna pattern.

Suggested Reading:

1. Skolnik, Merrill I, Introduction to Radar Systems, MGH, third edn., 2001.
2. Barton. David K, Modern Radar System Analysis, Aretech House, 1988.
3. Peebles PZ, ‘Radar Principles’, John – Willey, 2004.

EC 471 UE

GLOBAL NAVIGATIONAL SATELLITE SYSTEM

Instruction:	4 Periods per week
Duration of University Examination:	3 Hours
University Examination:	75 Marks
Sessional:	25 Marks
Credits	4

OBJECTIVES

- To get familiarize with Satellite based navigation.
- To understand the concept of Position fixing GPS.
- To introduce state of the art technique for comparing the positional accuracy.

UNIT I

GPS fundamentals: INS, Trilaiteration, Hyperbolic navigation, Transit, GPS principle of operation, architecture, operating frequencies, orbits, Keplerian elements.

UNIT II

GPS Signals: GPS and UTC Time, Signal structure, C/A and P-Code, ECEF and ECI coordinate systems and WGS 84 datum, Important components of receiver and specifications, link budget.

UNIT III

GPS Error Models: Ionospheric error, Tropospheric error, Ephemeris error, Clock errors, Satellite and receiver instrumental biases, Antenna Phase center variation, multipath; estimation of Total Electron Content (TEC) using dual frequency measurements, Various DOPs, UERE.

UNIT IV

Modernization and DGPS: Future GPS satellites, new signals and their benefits, principle of operation of DGPS, architecture and errors, Spoofing and Anti-spoofing.

UNIT V

Other Constellations and Augmentation systems: GLONASS, Galileo and IRNSS System. Relative advantages of SBAS, SBAS: Features and Principle of operation of Wide area augmentation system (WAAS) and GAGAN

Suggested Reading:

1. Hoffman-Wellenhof, B., H.Lichtenegger and Collins., J., "GPS Theory and Practice", Springer-Verlag Wien NewYork, 2008.
2. Misra, Pratap and Per Enge, "Global Positioning System: Signals, Measurements and Pelformance", Ganga- Jamuna Press, Linclon, Massachusetts, USA, 2001.
3. Bradford W, Parkinson and James J.Spilker Jr., " Global Positioning System: Theory and Application Volume I and II", American Institute of Aeronautics and Astronautics Inc., Washington DC

EC 472 UE

MULTI RATE SIGNAL PROCESSING

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

Objectives

- To design efficient digital filters that meet a required frequency response specification and utilize such filters as part of a system to alter the sampling rate of a signal
- To develop efficient polyphase implementations of sampling rate converters
- To design multi-channel filter banks to decompose a signal into subbands and then synthesize a full-band signal from the subband components
- To successfully complete a project utilizing a filter bank to achieve a specified objective

Unit – I

Review of fundamentals of Multirate Systems: Decimation by a integer factor D, Interpolation by a integer factor I, Sampling rate conversion by a rational factor I/D, Interconnection of building blocks, Polyphase representation, Multi stage implementation of sampling-rate conversion, Applications of Multirate systems.

Unit – II

Multirate Filter banks: Digital filter banks, Uniform DFT filter banks, Polyphase implementation of Uniform filter banks. Nyquist filters: Lth -band filters, half band filters, design of Linear-phase Lth band FIR filters.

Unit – III

Quadrature - Mirror Filter banks : Two Channel QMF structure and analysis, Alias free filter bank, Alias - free realization, Alias - free FIR QMF bank, Alias - free IIR QMF bank, perfect reconstruction (PR) two - channel FIR filter bank, Alias - free L - Channel filter bank.

Unit – IV

Polyphase Representation.Condition for Perfect Reconstruction. Cosine - Modulated L - channel filter banks, Multilevel filter banks - filter with equal and unequal passband widths.

Unit – V

Introduction to wavelet theory, wavelet transform, Definition and Properties, Introduction to multi dimensionalmultirate signal processing.

Suggested Reading

1. Mitra SK " *Digital Signal Processing. A Computer Approach*," TMH, 3/e, 2006.
2. Vaidyanathan PP "*Multirate Systems and Filter Banks*," Pearson Education.2008.
3. Bruce W. Suter, "*Multirate and Wavelet Signal Processing*," Volume 8, Academic Press,1998.

EC 473 UE

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (ELECTIVE –IV)

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks
Credits	4

Objectives

- To understand the basic operation of Programmable gate arrays
- To learn the architecture of various types of FPGAs
- To design a digital circuit and implement it on an FPGA

UNIT – I

Review of Logic Design, Implementation with NAND – NOR gates, designing with multiplexers, implementation of logic functions with look-up tables, minimization of combinational functions based on a) Circuit size, gates and literals i.e. space & power b) number of levels of logic i.e. time or circuit depth. The Quine-McCluskey Algorithm, Multi level logic minimization, covering, factored forms, technology mapping, review of finite state machines, one hot encoding

UNIT – II

Programmable Logic: Introduction, programmable logic devices (PLDs), SPLDs, CPLDs, fundamentals of PLD circuits, PLD symbology, PLD architectures: Progrmmable Read Only Memories (PROMs), Programmable Array Logic (PAL), ALTERA CPLDs

UNIT – III

FPGAs: Introduction, Programming Technologies: SRAM, Antifuse, EPROM and EEPROM Xilinx FPGAs, Actel, Altera, Concurrent Logic FPGAs. Crosspoint Solutions FPGA, translation to XNF format, Partition, Place and route, Technology mapping for FPGAs: Logic Synthesis, logic Optimization, Lookup Table Technology Mapping, Mapping into Xilinx 3000 CLBs, Multiplexer Technology, Mapping.

UNIT – IV

Logic Block Architecture: Logic Block functionality Versus area-efficiency, Impact of Logic Block Functionality in FPGA performance, Routing for FPGAs: Segmented Channel Routing, Routing for Symmetrical FPGAs, CGE detailed router Algorithm. Flexibility of FPGA routing architectures: Logic Block, Connection Block, Trade offs in Flexibilities of the S and C blocks, A theoretical model for FPGA routing.

UNIT – V

Platform FPGA architectures, Multi-FPGA Systems: Xilinx Virtex II Pro Platform FPGA, Altera Stratix Platform FPGA, Serial I/O, Memories, CPUs and Embedded Multipliers, Multi FPGA systems: Interconnecting Multiple FPGAs, partitioning, Novel architectures.

Suggested Reading:

1. Park K. Chan / SamihaMourad, "Digital Design using Field Programmable Gate Arrays", Pearson,1994 (Unit-I)
2. Ronald J Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems: Principles & Applications", 10th Edition, Pearson, 2009 (Unit-II)
3. Stephen Brown ZvonkoVranesic – Fundamentals of Digital Logic with VHDL design, McGraw Hill – 2000 (Unit I & II).

EC 474 UE

ADVANCED TOPICS IN MICROWAVES

Instruction	4 Periods per week
Duration of University Examination	3 hours
University Examination	75 Marks
Sessional	25 Marks
Credits	4

OBJECTIVES

- To learn strip line and micro-strip lines used in developing microwave systems.
- To introduce the microwave filters and transmission lines.
- To gain knowledge to analyze symmetrical four port networks using transmission and scattering matrices.

UNIT I

Impedance matching: Theory of small reflections, Multisection transformers. Binomial and Tchebyscheff transformers, Tapered Transmission lines, Exponential and triangular tapers.

UNIT II

Analysis of symmetrical four port networks, Even and odd mode analysis using transmission matrix and scattering matrix, Analysis of branch line coupler. Hybrid ring.

UNIT III

Introduction to strip and microstrip lines, characteristic impedance, propagation. field configuration, Coupled lines, Directional coupler using TEM mode coupled lines. Design.

UNIT IV

Passive microwave devices, reciprocal and nonreciprocal microwave components and their s-parametr s Faraday rotation, nonreciprocal components using Faraday rotation.working principle, construction characteristics and applications of isolator, circulator. phase shifters.

UNIT V

Periodic Structures and Filters, wave analysis of periodic structure; KO- diagrams, Filter design by insertion loss method, Power loss ratio, Maximally flat characteristics, Chebyshev filter, LP filter design, Frequency transformation.

Suggested Reading:

1. R. E. Collins, Foundations for Microwave Engineering, 2nd Edition, John Wiley.2001.
2. K. C. Gupta & A. Singh, Microwave Integrated Circuits, New Age, 1983.
3. M. L. Sisodia&G.S.Raghuwanshi, Microwave Circuits and Passive Devices, Wiley Eastern, 1987. 4. Pozar D,M., Microwave Engineering, John Wiley & Sons 3 id Edition, 2005.